A High Performance 1.5 dB Low Noise GaAs PHEMT MMIC Amplifier for low cost 1.5-8 GHz commercial applications

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ABSTRACT

A three stage, 1.5 to 8 GHz, 1.5 dB noise figure monolithic GaAs PHEMT has been designed, fabricated, and tested. This MMIC uses state-of-the-art .15u gate PHEMT devices, self-biasing current sources, source follower interstage, resistive feedback, and on-chip matching to make a unique low noise amplifier. Typical gain of 21 dB, VSWR of 2:1, and P-1dB output power of 7dBm have been measured. The die area is small (0.40 mm sq.) and is compatible with surface mount packages. DC power requirements are low, consuming only 14mA from a single +5V supply. This MMIC LNA has the best combination of noise figure, gain, low current, match, wide bandwidth, and low cost of any advertised or published product to date.

INTRODUCTION

There are numerous commercial bands from 1.5 to 8.0 GHz, some mature, many emerging. These bands include 1.5 GHz (GPS), 1.9 GHz (PCN), 2.1 GHz (MMDS), 2.4 GHz & 5.7 GHz (ISM), 3.7 to 4.2 GHz (satellite/TVRO), C-Band (Aviation, medical), and full 1.5 to 8.0 GHz band (Instrumentation). A Monolithic Microwave Integrated Circuit (MMIC) Low Noise Amplifier (LNA) has been designed to help those system designers involved at these frequencies. It includes integrated bias and impedance matching, eliminating most of the 10 to 15 components required to implement a comparable discrete design. The MMIC LNA's price and performance is comparable to a discrete-on-PC board design while adding smaller size and easier system design. A low cost surface mount package is utilized to maintain performance and simplify application. This MMIC LNA is available now as the Hewlett-Packard CMCD MGA-86576 for low cost (< $10) applications.

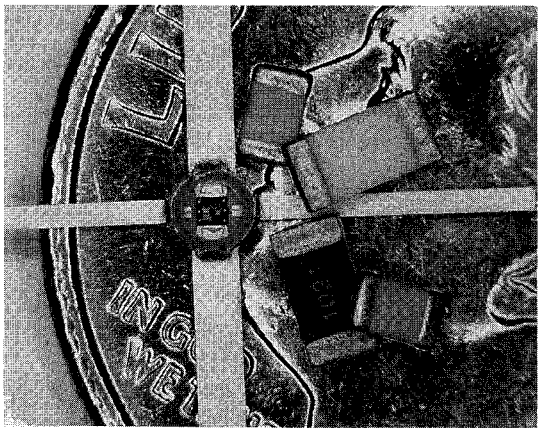

Figure 1. All the components, resting on a dime, required to build a low noise amplifier using a GaAs PHEMT MMIC in a surface mount package.

DEVICE AND FABRICATION

This monolithic low noise MMIC amplifier employs Hewlett-Packard's advanced PHEMT (Pseudomorphic High Electron Mobility Transistor)*1 process for 0.25 dB noise figure (at 4.0 GHz). The devices are built using MBE (Molecular Beam Epitaxy) material growth techniques. The gates are defined using electron-beam lithography. Typical lengths range from 0.12 to 0.17 microns. A mushroom shaped gate is used in order to reduce gate parasitic resistance by increasing the gate's cross sectional area. Stepper lithography is used to define all layers not directly written. The combination of MBE and stepper masking ensures high uniformity and consistency across a wafer and wafer to wafer.

The design's primary amplification devices consist of a interdigitated 300 um structures. These FETs are made of a single gate feed branching into four parallel gate fingers 75 um long. Typically these devices exhibit an Idss of 105 mA (0.35A/mm), a pinch off voltage of -0.9V and a transconductance of 100 mS (330 S/mm).

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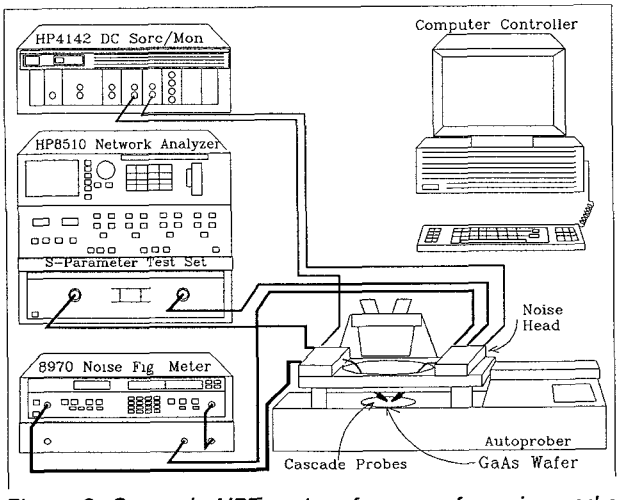

Figure 2. Cascade NPT system for on-wafer noise and s-parameter measurements of FETs and MMICs.

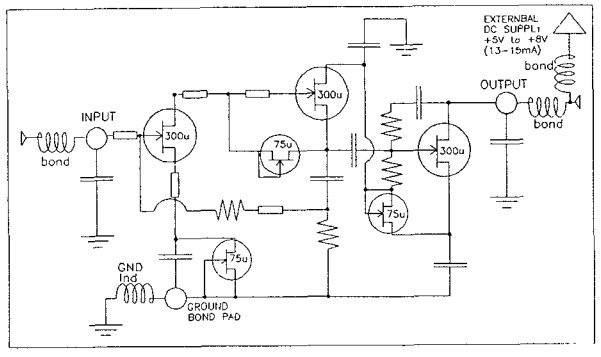

Figure 3. Circuit schematic of the MMIC LNA.

From measured on wafer I-V curves and s-parameters, a small signal equivalent model was constructed. In addition, a library of noise and s-parameters were measured (5% to 40% of Idss) on the Cascade Noise Parameter Test system [1].

The design uses a patented GaAs FET 75 um current source as a saturated resistor for bias and RF choke [3, 4]. The current source consists of a single finger PHEMT with the gate and source connected together. The devices typically have a saturation of 14 mA and provide a -0.7V offset. Final noise and s-parameters for the device are determined through on wafer probing.

In addition to these active devices, the monolithic design makes use of bond wires for source grounding, air-bridges for interconnect, and MIM capacitors using silicon nitride for RF grounding and DC blocking. Resistors are built using the native 330 ohms/square bulk active material resistance.

MONOLITHIC LOW NOISE AMPLIFIER DESIGN

As with most MMIC designs today, this LNA was designed through extensive use of computer aided design techniques. Libra [6] and HP MDS [7] were both used to simulate RF and DC performance of the components and the entire circuit. All measured data for models and simulation was obtained through automated test. DC and RF data were collected using an HP 8510C Automatic Network Analyzer, an HP4142 DC parametric analyzer, an HP 8970B noise figure test system, and various support equipment. See figure 2 for a typical setup. Software used to make automated measurements included custom software, Cascade Microtech's NPT [9], and HP IC-CAP [8]. All components are measured and modeled under many conditions and the data is stored and referenced in a library. Artwork for the MMIC is generated using AutoCAD [10], and Mentor Graphics.

Several different CAD tools and separate models are used to ensure that the simulated performance is not the figment of some software's imagination. The physical layout is correlated to the simulation elements, including coupling, unwanted feedback, an a removed ground reference plane. Also, utilizing varying parameters for lumped elements (corresponding to process variation) provides one with a design that is high yielding.

Figure 3 presents a lumped element schematic of the PHEMT MMIC LNA as fabricated. The MMIC LNA consists of two primary FET gain stages, one source follower stage, three current sources, two resistive feedback networks, bias resistors, and two source capacitors. Each 12 dB gain stage, and unity gain source follower stage, consists of a PHEMT FET biased at 15% of Idss with the use of a current source attached to the FET source. The voltage drop across the current source is used to set the FETs gate-to-source voltage, thus its bias value. Process variations affect both FET and current source equally. In this manner a constant percentage of Idss is maintained, preserving noise figure, gain, and match. This results in a robust design tolerant of the natural variation inherent in the fabrication process.

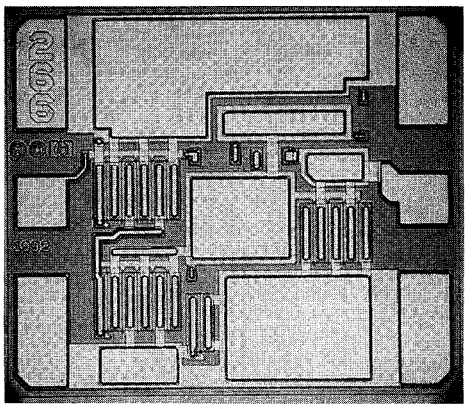

Figure 4. Micro-photograph of the MMIC LNA

This topology utilizes a source follower to provide unity gain and impedance transformation for an internal feedback point. The interstage-to-input resistive feedback is very light, used to improve stability and input VSWR. This feedback does degrade the noise figure above the discrete PHEMT minimum value (approximately 0.5 dB), but the reduction of the magnitude of both Gamma Opt and S11 is worth the price. An added benefit is improved stability.

The last stage of the MMIC provides more gain, output power, and output match. A series capacitor and resistor network provides medium feedback on the last stage to improve match, provide stability, and flatten gain. The source capacitors on the gain stages allow for a single DC supply, and provide high pass filtering. Four internal capacitors are used for DC blocks. This topology results in the elimination of inductors, saving space and the associated yield loss.

The MMIC LNA is very compact The die is 0.59mm (23 mils) by 0.68mm (27 mils). The design is GSG probable for on-wafer DC and RF evaluation. A photograph of the MMIC is shown in Figure 4.

A package must be known and characterized if it is to be used with a MMIC. All packages affect the performance of the device. Figure 5 shows the model of the package used for this MMIC. As seen, the package introduces a new level of parasitics and feedback to the device. However, this MMIC takes into account package parasitics, while maintaining stability and performance.

RESULTS

Figures 6, 7, and 8 illustrate typical performance of more than 500 packaged parts. In a 50 Ohm system at

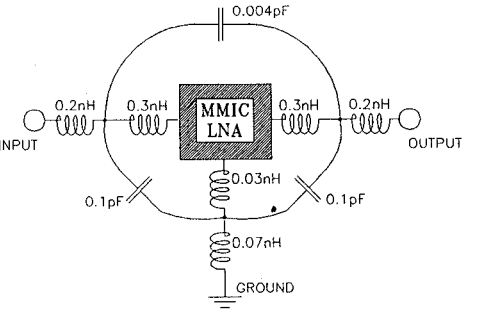

Figure 5. Model of the surface mount package used.

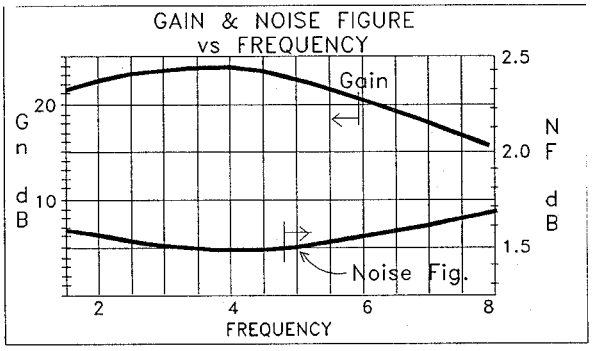

Figure 6. Typical minimum noise figure and associated gain for the MMIC LNA.

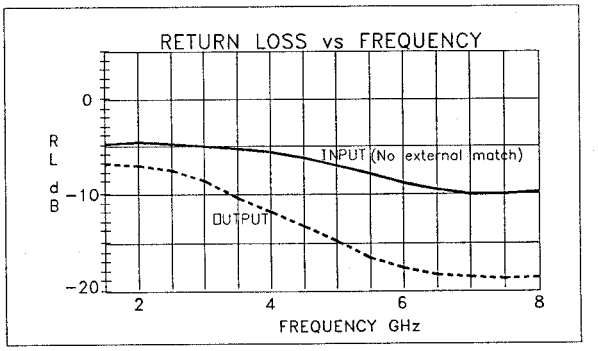

Figure 7. Typical MMIC LNA input & output return loss.

4.0 GHz the typical gain is 21 dB and typical noise figure is 1.9 dB. The input return loss is 6.0 dB while the output return loss is better than 10.0 dB. Typical output power at one dB compression is greater than +7 dBm with +7.0 V applied to the output. The performance can be improved for a narrow frequency band (about 15%) with a simple external input match (series inductance of .1 to 2 nH). Such a match produces a minimum noise figure of 1.5dB, gain greater than 22 dB, and input return loss better than 15.0 dB.

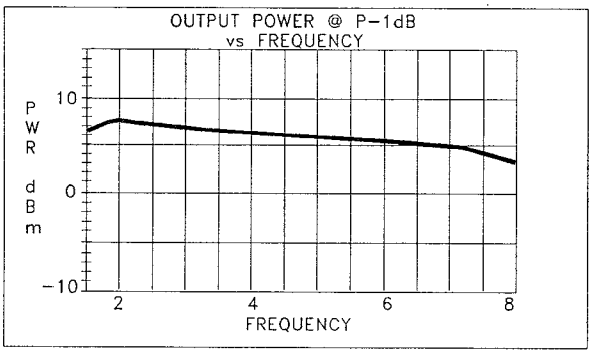

Figure 8. Typical MMIC LNA output power at P-1dB.

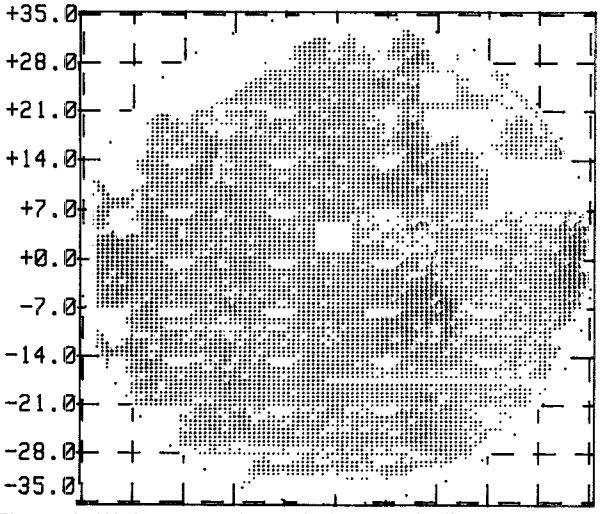

Figure 9. Wafer map where dark areas indicate functional die. Yield is uniform and high.

A 5 volt DC supply can be used since the PHEMT process exhibits high gain at low Vds. All stages share the current, thus the MMIC consumes typically only 14mA, 1/3 less than any known comparable devices. Figure 9 demonstrates the high yield across a wafer. Figure 10 demonstrates the extreme uniformity that this topology provides.

APPLICATION

The MMIC requires only a 5.0V supply, (7.0 V for optimum power and noise results). As figure 11 shows, external elements required for the MMIC are an RF choke, an output blocking capacitor, and an optional input series inductor to center noise and return loss at a desired frequency. The input is at ground and should be DC blocked if bias is on the RF line. The MMIC utilizes a surface mount package, able to be easily mounted on a variety of board types. This MMIC is stable over all commercial temperatures and has proven reliability.

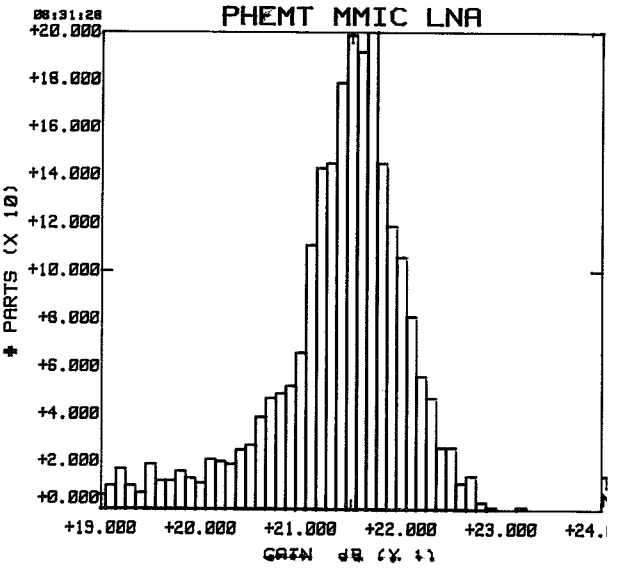

Figure 10. Distribution of gain on 5000 measured parts.

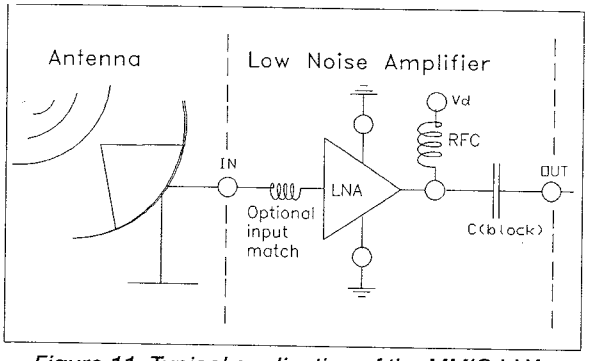

Figure 11. Typical application of the MMIC LNA.

ACKNOWLEDGMENTS

The authors wish to thank John Coward, Ruben Reyes, Ding Day, K.Y. Ramanujam, Gary Carr, Craig P. Snapp for their support and assistance.

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6. LIBRA is trade mark and product of EEsof, Inc. Westlake Vilage, CA
7. MDS (Microwave Design System) is a product of Hewlett-Packard, Palo Alto, CA
8. IC-CAP Nonlinear model extraction software is a product of Hewlett-Packard.
9. NPT (Noise Parameter Test) is a product of Cascade Microtech, Beaverton, OR.
10. AutoCAD is a product of AutoDesk, Inc., Sausalito, CA.